In the Claims

Applicant has submitted a new complete claim set showing amended claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 1, 5-8, 10 and 11 as noted below.

1. (Currently Amended) A method of identifying an inaccurate model of a hardware circuit comprising the steps of:

~~simulating~~ running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level ~~to provide a set of expected results~~;

replacing the at least one abstract data type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

~~resimulating~~ re-running the model ~~with~~ by applying said expanded set of signals to the model to obtain a second set of results; and

comparing the ~~two sets~~ first set of expected results with the second set of results and providing an output signal indicating ~~if~~ that the model is inaccurate if the first set of expected results and the second set of results contradict.

2. (Original) A method as claimed in claim 1, wherein the model is an HDL model.

3. (Original) A method as claimed in claim 2, wherein said plurality of signals are selected from a standard logic package data set comprising one or more simple logic levels and one or more abstract data type levels.

4. (Original) A method according to claim 3 further comprising the step of, when said abstract data type is an X selected from the standard logic package, expanding each X into a 0 and a 1.

5. (Currently Amended) A method as claimed in claim 3, wherein the ~~or each~~ at least one abstract data type level ~~signal~~ is converted into two simple logic signals.

6. (Currently Amended) A method according to claim 1, further comprising the steps of, during a process of verifying the accuracy of the model, said model being a digital model, comparing the results of the model with ~~the~~ results from ~~the simulation of~~ running an analog model of the circuit, identifying whether the digital model is an accurate model and only comparing the digital model results with the analog model results if the digital model is determined ~~in said comparing step~~ to be accurate.

7. (Currently Amended) A method according to claim 6, in which said analog model is a SPICE model of the hardware circuit ~~test cell~~.

8. (Currently Amended) A method according to claim 1, further comprising the steps of during running the model ~~simulation for the plurality of signals~~ determining the value of each output from said model; and

during ~~resimulation~~ re-running the model determining for the expanded set of signals the value of each output from the model.

9. (Previously Presented) A method as claimed in claim 1, wherein said model is a digital model.

10. (Currently Amended) A system for identifying an inaccurate model of a hardware circuit comprising:

means for ~~simulating~~ running the model of the circuit by applying a plurality of signals to the model to obtain a first set of expected results, said plurality of signals having at least one abstract data type level ~~to provide a set of expected results~~;

means for replacing the at least one ~~or each~~ abstract data ~~tpe~~ type level with two or more levels having different values to thereby provide an expanded set of signals to apply to said model;

means for ~~resimulating~~ re-running the model by applying ~~with~~ said expanded set of signals to the model to obtain a second set of results; and

means for comparing ~~the two sets of~~ the first set of expected results ~~and~~ with the second set of results and providing an output signal indicating ~~if~~ that the model is inaccurate if the first set of expected results and the second set of results contradict.

11. (Currently Amended) A system as claimed in claim [[9]] 10, wherein said system is a computer system.

12. (Previously Presented) A computer program comprising program code that, when executed on a computer, performs any of the steps of any of claims 1 to 9.